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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,580	07/23/2003	Daniel Kenneth Lunecki	CYGL-26,370	7734

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
05/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@dalpat.com

Office Action Summary	Application No.	Applicant(s)	
	10/625,580	LUNECKI ET AL.	
	Examiner	Art Unit	
	KIM T. HUYNH	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 4th of February 2008 for a request for continued examination (RCE) under 37 CFR 1.114 based on the application No. 10/625580, which the request is acceptable and an RCE has been established. Currently, claims 1-21, 23-30 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 16-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacon (US Patent 6,307,538) in view of Nilsson et al. (US Patent 6,189,052)

As for claim 16, Bacon teaches a modularized serial data module for interfacing between a first serial data communication interface (see figure 3, microcontroller core 102, SIE 104), operating in accordance with a first serial data protocol from and to an external device for transmitting and receiving serial data that transmits/receives data and also provides power to the modularized serial data module (see figure 3, and column 5 lines 6-12), and a second serial data communication interface operating in accordance with an associated serial data protocol that transmits or receives data (see figure 3, isolator 92 and column 5

lines 1-5), comprising: a connector housing for providing a physical interface with the first serial data communication interface (see figure 3, connector housing, a data interface for providing a physical interface with the second serial data communication interface (see figure 3, isolator 92); a processor housing disposed adjacent said connector housing and interfacing therewith (see figure 3, microcontroller core 102; a single chip processor disposed within said processor housing, said processor operating with a native digital processor protocol different from said at least one of said first or second serial data protocols, and said processor also operable to be powered by the serial data communication interface through said connector housing (see figure 3, microcontroller 102 and column 5 lines 5-12), and said processor also operable to interface with the data portion of the first serial data communication interface through said connector housing (see figure 3, SIE 104 and column 5 lines 5-13), and to interface with the data portion of the second data communication interface through said data interface (see column 4 lines 55-67)., and wherein said single chip processor is operable to provide processing of information based upon data received from either the first serial data communication interface in the first serial data protocol through said connector housing or the second serial data communication in the second serial data protocol through said data interface, or processing information for transmission to either the serial data communication interface in the first serial data protocol through said connector housing or the second serial data

communication interface in the second serial data protocol through said data interface (see figure 3 and column 5 lines 6-12).

Bacon discloses all the limitations as the above except and operating on a second time base different from said first time base such that said transmission is asynchronous, wherein said processor receives the serial data generated with the second time base and converts the data to the native protocol with clock recovery. However, Nilsson discloses provide i/o processor supporting for running at a high clock frequency with different protocols. Data transferring in the RS-232 interface can work in synchronous and asynchronous mode with clocking frequency. (col.3, line 24-col.4,line 26) Furthermore, I/O processor reprogrammable to any general i/o protocol with UART(universal asynchronous receiver transmitter) to convert serial to parallel data and vice versa. (col.5, lines 22-59)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Nilsson's teaching into Bacon's system so as to provide an improved input/output control system supporting different protocols. (col.1, lines 65-67)

As for claims 17-19, Bacon teaches wherein said data interface comprises an analog interface (see column 4 lines 30-33).

As for claims 20-22, Bacon teaches wherein said data interface comprises

a digital data interface (see column 5 lines 6-12).

As for claims 23, Bacon teaches wherein the first serial data protocol is a synchronous data protocol (see column 6 lines 29-30).

As for claims 24, Bacon teaches wherein the first serial data protocol is associated with a universal serial bùs data protocol (see column 3 lines 47).

As for claim 25, Bacon teaches wherein processor utilizes a free running time base generated within said connector housing (see column 6 lines 22-31).

4. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacon (US Patent 6,307,538) in view of Ware et al. (US Patent 5,446,696) and further in view of Nolan et al. (US Patent, 5,841,996) and further in view of Nilsson et al. (US Patent 6,189,052)

As for claim 1, Bacon teaches a modularized serial data module for interfacing with a serial data communication interface to an external device operating in accordance with a first serial data protocol that transmits/receives data and also provides power to the modularized serial data module (see figure 3, microcontroller core 102 and column 5 lines 6-12), comprising: a connector

housing for providing a physical interface with the serial data communication interface (see figure 3,connector plugs 106, SIE 104)., a processor housing disposed adjacent said connector housing and interfacing therewith (see figure 3, microcontroller 102)., a single chip processor disposed within said processor housing and operable to be powered by the serial data communication interface through said connector housing and also operable to interface with the data portion of the serial data communication interface through said connector housing, said processor operating with a native digital processor protocol different that said first serial data protocol (see figure 3, microcontroller 102, power supply 184, ground 182, and column 5 lines 6-18)', and wherein said single chip processor is operable to provide processing of information based upon data received from the serial data communication interface with the first serial data protocol through said connector housing or processing information with the first serial data protocol for transmission to the serial data communication interface through said connector housing (see figure 3 and column 5 lines 5-18).

Bacon does not explicitly teach oscillator disposed with the processor housing. However, Ware teaches an oscillator disposed within a processor(see figure 5, oscillator 565 disposed within the processor 560). Therefore, it would have been obvious to a person of an ordinary skill in the ad at the time the invention was made to have combined the teachings of Ware into the teachings of Bacon because the oscillator will providing control of frequency for refresh

signal thus power reduction can be reduced significantly (see abstract and column 3 lines 49-52).

Furthermore, the modified of Bacon discloses all the limitations as above except whether this oscillator disposed on a processor chip a free running oscillator that required no external reactive components for the operation thereof, which said oscillator provides an operating clock signal to said processor for operation thereof, wherein said free running oscillator operates on said first time base which is completely generated one chip with said single chip processor. However, Nolan discloses a microcontroller includes watchdog timer that is realized as a free running on-chip RC oscillator which does not require any external components. (col.5, lines 4-11) Therefore, it would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Nolan's teaching into the modified of Bacon's system so as to provide the capability for programming a microcontroller while in its end-use application. (col.1, lines 59-61)

The modified system of Bacon discloses all the limitations as the above except and operating on a second time base different from said first time base such that said transmission is asynchronous, wherein said processor receives the serial data generated with the second time base and converts the data to the native protocol with clock recovery. However, Nilsson discloses provide i/o processor supporting for running at a high clock frequency with different protocols. Data transferring in the RS-232 interface can work in synchronous and

asynchronous mode with clocking frequency. (col.3, line 24-col.4,line 26) Furthermore, I/O processor reprogrammable to any general i/o protocol with UART(universal asynchronous receiver transmitter) to convert serial to parallel data and vice versa. (col.5, lines 22-59)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Nilsson's teaching into Bacon's system so as to provide an improved input/output control system supporting different protocols. (col.1, lines 65-67)

As for claim 2, Bacon teaches a data interface between said processor in said processor housing and external to said processor housing for transmission of data from the processor exterior to the processor housing or receipt of data generated exterior to said data housing for processing by the said processor (see figure 3).

As for claims 3-5, Bacon teaches wherein said data interface comprises an analog interface (see column 4 lines 30-33).

As for claims 6-8, Bacon teaches wherein said data intedace comprises a digital data interface (see column 5 lines 6-12).

As for claim 9, Bacon teaches a transducer disposed in said processing

housing for interfacing between said processor and exterior to said processor housing for receipt of external information generated external to said processor housing or providing of information to the exterior of said processor housing, said transducer interfaced with said processor (see figure 3, transducer 80, 82, 84).

As for claim 10, Bacon teaches wherein said transducer is operable to sense exterior information for input to said processor for processing thereof and subsequent transmission to the serial data line through said connector housing (see figure 3, transducer 80, 82, 84).

As for claim 11, Bacon teaches wherein said transducer is operable to generate information for output exterior of said processor housing (see figure 3).

As for claim 12, Bacon teaches wherein said transducer requires power and the power required thereby is provided through said connector housing and said processor housing (see figure 3 and column 5 lines 13-18).

As for claim 13, Bacon teaches wherein the first serial data protocol is a synchronous data protocol (see column 6 lines 29-30).

As for claim 14, Bacon teaches wherein the first serial data protocol is

associated with a universal serial bus data protocol (see column 3 lines 47).

Response to Amendment

5. Applicant's amendment filed on 2/4/08 have been fully considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that the prior arts do not disclose and operating on a second time base different from said first time base such that said transmission is asynchronous, wherein said processor receives the serial data generated with the second time base and converts the data to the native protocol with clock recovery. However, Nilsson discloses provide i/o processor supporting for running at a high clock frequency with different protocols. Data transferring in the RS-232 interface can work in synchronous and asynchronous mode with clocking frequency. (col.3, line 24-col.4,line 26) Furthermore, I/O processor reprogrammable to any general i/o protocol with UART(universal asynchronous receiver transmitter) to convert serial to parallel data and vice versa. (col.5, lines 22-59) Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

Conclusion

6. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to*

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at (571)272-3632 or via e-mail addressed to [mark.rinehart@uspto.gov].

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

/K. T. H./

Examiner, Art Unit 2111

/Khanh Dang/

Primary Examiner, Art Unit 2111